Claims

1. A method of coupling

    at least one (conventional) unit processing data in a se-
    quential manner, e.g. a CPU, von-Neumann-Processor and/or
    microcontroller,

         the (conventional) unit for data processing compri-
    sing an instruction pipeline,

     and

    an array for processing data comprising a plurality of data
    processing cells, e.g. a preferrably coarse grain and /or
    preferrably runtime reconfigurable data processor, FPGA,
    DFP, DSP, XPP or chaemeleon-technology-like data processing
    fabric,
    wherein the array is coupled to the instruction pipeline.

2. A method in particular according to claim 1, wherein the
    input and /or output between the at least one (conventional
) unit processing data in a sequential manner, e.g. a CPU,
    von-Neumann-Processor, microcontroller, and
    an array for processing data comprising a plurality of data
    processing cells, e.g. a runtime and/or reconfigurable data
    processor, DFP, DSP, XPP or chaemeleon-technology-like data
    processing fabric,
    wherein data is transferred via at least one data path
    being provided therebetween comprising at least one FIFO so
    as to allow for a less tight coupling and /or data proces-
    sing within the at least two units that is not strictly
    synchroneous.

3. A method according to any of the previous claims wherein
    data is transferred via at least one data path that allows
    for transfer of data between units not being transferred
    through a register.

4. A method according to any of the previous claims wherein a path for the transferral of status information and/or event information such as flags, overflow, carry and the like is provided between the (conventional) unit for data processing and the at least one array for processing data.

5. A device for processing data comprising at least one (conventional) unit processing data in a sequential manner, e.g. a CPU, von-Neumann-Processor and/or microcontroller,
   the (conventional) unit for data processing comprising an instruction pipeline,
   and
   an array for processing data comprising a plurality of data processing cells, e.g. a runtime and/or reconfigurable data processor, DFP, DSP, XPP or chaemeleon-technology-like data processing fabric,
   wherein the array is coupled to the instruction pipeline.

6. The device according to the previous claim wherein
   at least one data path is provided between the array and the conventional processor comprising at least one FIFO so as to allow for a less tight coupling and /or data processing within the at least two units that is not strictly synchroneous
   and /or wherein
   at least one data path is provided that allows for transfer of data not being transferred through a register.

7. A method of at least one (conventional) unit processing data in a sequential manner, e.g. a CPU, von-Neumann-processor, microcontroller, being preferrably adapted for data processing to any of the previous methods and or according to a previously claimed devices
   the (conventional) unit for data processing prefer-

rably comprising an instruction pipeline   and
an array for processing data comprising a plurality of data
processing cells, e.g. a runtime and/or reconfigurable data
processor, DFP, DSP, XPP or chaemeleon-technology-like data
processing fabric, wherein a path allowing for block data
transfer is provided from the data cache and /or other data
source and the array.

8. A method of data processing using an aray of data proces-
    sing elements wherein input data to be processed are dupli-
    cated prior to processing.

9. A method according to the previous claim wherein the input
    data to be processed are duplicated
    by connecting a plurality of operand or other inputs to an
    input source such as the output of a data processign unit
    upstream in the data stream or
    by using a unit storing and /or latching and /or holding
    said input data, the unit being within the data path and
    /or fanning out the data to a number of different inputs.

10. A method of data processing using an array of data proces-
    sing elements reconfigurable at runtime, said data proces-
    sing being effected by a plurality of configurations,
    wherein the amount of time allowed for running one configu-
    ration is limited.

11. A method of preparing an array for processing data reconfi-
    gurable at run time wherein a number of instructions is
    combined to form a number of configurations to be run one
    after the other and /or in parallel on said array and
    wherein an execution time of a single configuration is re-
    stricted, in particular when repeated operations are to be
    performed such as loops and/or iterations.